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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/647,664 | 08/25/2003 | Tony Mai | 2037.2038-001(11067-01US- | 2135 |

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| EXAMINER | |
|---|---|
| BAYARD, EMMANUEL | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2611 | |

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/647,664 | MAI, TONY | |
| | Examiner | Art Unit | |
| | Emmanuel Bayard | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimura et al U.S. Patent No 5,994,934.

As per claim 1, Yoshimura et al teaches a delay locked loop (see figs. 1 and 9) comprising: a delay circuit which provides a delay to a reference clock (see fig.9 element CLKIN) to generate a feedback clock (see fig.9 element FBCLK), the delay circuit having a delay range; a phase detector which compares phase of the reference clock and the feedback clock to change the delay of the delay circuit (see fig.9 element 3); and an initialization circuit (see fig.9 element 13) that after reset of the delay locked loop assures that the phase detector initially changes the delay in a direction away from a first end of the delay range after receipt of one of the reference clock and feedback clock (see abstract and col.3, lines 60-67 and col.4, lines 5-25) and enables a change in the delay in an opposite direction (see col.4, lines 57-58) toward the first end only after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock (see col.4, lines 57-67 and col.5, lines 53-57).

As per claim 2, Yoshimura et al teaches 1 wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay

and the opposite direction towards the first end decreases the delay (see col.5, lines 6-12 and col.6, lines 54-67 and col.7, lines and col.8, line 67-col.9, lines 5).

As per claim 3, Yoshimura et al teaches wherein the initialization circuit increases the delay after receipt of the reference clock and enables decrease in the delay only after receipt of the reference clock followed by the feedback clock (see col.2, lines 28-55 and col.3, lines 15-34).

As per claim 4, Yoshimura et al teaches wherein the initialization circuit comprises: a first latch (see fig.10 element 52) responsive to the reference clock (see fig.10 element CLKIN) which detects a first edge of the reference clock to enable change in the delay in the direction away from the first end; and a second latch (see fig.10 element 57) responsive to the feedback clock (see fig.10 element FBCLK) which detects an edge of the feedback clock after the first edge of the reference clock has been detected by the first latch to enable change in the delay in the opposite direction, the input of the second latch coupled to the output of the first latch (see col.13, lines 15-67).

As per claim 5, Yoshimura et al teaches wherein the initialization circuit further comprises: a third latch (see fig.10 element 53) responsive to the reference clock (see fig.10 element CLKIN) which detects a next edge of the reference clock to delay enabling change in the delay in the first direction for at least one reference clock period, the input of the third latch coupled to the output of the first latch; and a fourth latch (see fig.10 element 58) responsive to the feedback clock (see fig.10 element FBCLK) which detects a next edge of the feedback clock to delay the enabling of change in the delay

in the opposite direction for at least one feedback clock period, the input of the fourth latch coupled to the output of the third latch (see col.13-col.14).

As per claim 6, Yoshimura et al teaches wherein the first edge of the reference clock is a rising edge and the edge of the feedback clock is a rising edge (see col.2, lines 33-48 and col.9, lines 55-57 and col.10, lines 10-30).

As per claim 7, Yoshimura et al teaches wherein the initialization circuit comprises: a first latch (see fig.10 element 52) responsive to the feedback clock (see fig.10 element FBCLK) which detects a first edge of the feedback clock to enable change in the delay in the direction away from the first end; and a second latch (see fig.10 element 56) responsive to the reference clock which detects an edge of the reference clock after the first edge of the feedback clock has been detected by the first latch to enable change in the delay in the opposite direction, the input of the second latch coupled to the output of the first latch (see fig.10).

As per claim 8, Yoshimura et al teaches wherein the phase detector comprises: a latch responsive to the reference clock to generate a first phase control signal (see fig.2 element 4U); and another latch responsive to the feedback clock to generate a second phase control signal (see fig.2 element 4D).

As per claims 9 and 13, Yoshimura et al teaches method for initializing a delay locked loop comprising the steps of: providing a delay to a reference clock (see fig.9 element CLKIN) to generate a feedback clock (see fig.9 element FBCLK), the delay circuit being initially set at a first end of a delay range; comparing phase of the reference clock and the feedback clock to change the delay of the delay circuit (see fig.9 element

3); after reset of the delay locked loop assuring that the delay initially be changed in a direction (see abstract and col.3, lines 60-67 and col.4, lines 5-25) away from the first end of the delay range after receipt of the reference clock; and enabling a change in the delay in an opposite direction toward the first end only after receipt of the reference clock followed by receipt of the feedback clock (see col.4, lines 57-67 and col.5, lines 53-57).

As per claim 10, Yoshimura et al teaches wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay (see col.5, lines 6-12 and col.6, lines 54-67 and col.7, lines and col.8, line 67-col.9, lines 5).

As per claim 11, Yoshimura et al teaches further comprising the steps of: delaying enabling adjustment of the delay in the first direction until a first predetermined number of the reference clock edges are detected; and delaying enabling adjustment in the opposite direction until a second predetermined number of the reference clock edges are detected (see col.2, lines 33-48 and col.9, lines 55-57 and col.10, lines 10-30 and see col.13, lines 15-67).

As per claim 12, Yoshimura et al teaches wherein the first edge of the reference clock is a rising edge and the edge of the feedback clock is a rising edge (see col.2, lines 33-48 and col.9, lines 55-57 and col.10, lines 10-30).

As per claim 14, Yoshimura et al teaches phase detection circuit for comparing phase of a first and second input signals (see figs 1-2, 9 element 3) comprising: a first latch responsive (see fig.2 element 4U) to the first input signal to generate a first phase

control signal; a second latch responsive (see fig.2 element 4D) to the second input signal to generate a second phase control signal; an initialization circuit (see fig.9 element 13) that enables the first latch after receipt of one of the first and second input signals and enables the second latch only after receipt of the one of the first and second input signals followed by receipt of the other of the first and second input signals (see abstract and col.3, lines 60-67 and col.4, lines 5-25 and (see col.4, lines 57-67 and col.5, lines 53-57).

As per claim 15, Yoshimura et al teaches, wherein the initialization circuit enables the first latch after receipt of a first plurality of said one of the first and second input signals and enables the second latch only after enabling the first latch and the receipt of a second plurality of said other of the first and second input signals (see fig.10 and col.13-col.14).

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al U.S. Patent No 6,731667 B1 teaches a zero-delay circuit.

Lee U.S. Patent No 6,437,818 B1 teaches a delay locked loop.

Von Kaenel U.S. Patent No 6,642,762 B2 teaches a method and apparatus to ensure DLL locking.

Mnich U.S. Patent No 6,346,839 B1 teaches a low power consumption integrated circuit.

Merritt U.S. Patent No 6,556,643 B2 teaches a majority filter.

Wu et al U.S. Patent No 6,100,736 teaches a frequency doubler using DLL.

Ooishi et al U.S. patent No 6,166,990 teaches a clock reproduction circuit (*).

Matsuzaki et al U.S. Patent No 6,088,255 teaches a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Bayard
Primary Examiner
Art Unit 2611

10/6/06

EMMANUEL BAYARD
PRIMARY EXAMINER